



Course Overview & Table of Contents

	Day 1	Day 2	Day 3	Day 4	Day5
9.15 10.45	1.1 Semiconductor Basics PN junctions NPN Bipolar formation	2.1 CMOS Modelling Threshold Voltage Device Equations Large Signal Models	3.1 Amplifiers: 1 & 2 tr amplifiers; Frequency Response; CMOS vs BiCMOS	4.1 Passives: R, L, C Matching: Centroiding, .	5.1 CMOS Logic Types; Fanout; Metastability T _j ; Pwr Diss; θ_{ja} ESD Maps
Break					
11.15 12.45	1.2 MOS Devices CMOS processes Oxidation Diffusion/Implantation	2.2 Small-Signal Models; 2nd Order Effects SPICE models & accuracy	3.2 Cascodeing; Diff Amps; OTA; PSRR/CMRR	4.2 Filters: gmC, mosC Filters: Switched Capacitor Circuits	5.2 Yield; Reliability; Deep Sub-Micron Manufacturability Halo/STI effects
Break					
2.00 3.30	1.3 LAB SIMPLer Mask Layout &Process Design-NPN &dual Gate Ox NMOS	2.3 LAB Schematic Entry; MOS I-V SPICE Simulation	3.3 LAB SPICE Inverter Amplifier simulations: Gain, BW, delay sims	4.3 LAB Inverter Layout; LVS;DRC	5.3 LAB Diff Amp Layout; Matching, Interdigitating
Break					
4.00 5.30	1.4 Photolithography; Back-End processing: Metal, Dielectrics, Etching	2.4 CMOS Subcircuits: Switches; lev-shift; Current Sources I & V References	3.4 2-Stage Amplifier Low-Voltage deep sub micron analog design	4.4 Noise & Crosstalk in mixed-signal systems	5.4 LAB cont'd OP-Amp design cont;d - Gain, Offset, freq response, 1